High Speed Interconnect Solutions
Fibre Channel “Quadsplitter”

Test Report
Sabritec P/N 029900-3011
@1.0625 Gbps
Eye Patten and Jitter

Written by: _____

1 Scope

In current Fibre Channel systems, greater demand is put on cable and connector designers to address the high data rates already here and the ones fast approaching. At the moment, cable suppliers have produced excellent cable with tight tolerance characteristic impedance and low insertion loss. Connector suppliers, on the other hand, have been slower to respond to the need. The reason is in the unfamiliar interfacing. The most important concerns of users are the characteristic impedance and low reflection controls. Design equations for shielded differential pair lines exist but only in symmetrical-filled medium configurations, and they become inaccurate at cable entries. This is solvable with finite-element analysis where mixed mediums are calculable.

The high-speed data rates require transmission systems that minimize reflections and can only be achieved through controlled characteristic impedance from source to load. In microwave systems, this is accomplished with waveguide or coaxial transmission lines. In both cases, the line geometry is the determining factor along with dielectric and conductor materials. Steps, bends, protrusions and so on will invariably cause reflections with subsequent loss of transmission efficiency. In two-wire differential-mode transmissions, this is acceptable at lower data rates. However, when data rates become higher, such as with Fibre Channel (into microwave frequencies), the line characteristic impedances become much more critical.

Impedance

In these systems, the source and load differential impedances are usually high (100 to 150 O). Achieving these high impedances in coaxial transmission lines and connectors is size-prohibitive. As a result, a line configuration such as twinaxial where the signals carried between a pair of conductors (usually round) critically spaced from each other and surrounded by a conductive enclosure is used. In this "differential line," high impedances are more readily obtained because the mutual capacitance between the conductors is minimized, and differential impedance is approximately twice the pin-to-ground impedance.

Ideally, a matched system requires that the line characteristic impedance be equal to the source and load impedances. This condition is somewhat compromised in a connector, especially at the cable entry. Despite these conditions, excellent impedance control can be achieved by choosing constant diameter and effective dielectric-constant regions, setting these up as separate transmission line sections and applying the appropriate equations. This should yield predictable characteristic impedances. It is incumbent on the connector designer to configure his cable entry and contact spacing to avoid excessive flaring out of the cable conductors. Proper choice of cable and compensation techniques greatly reduces the effect of flaring.

Quadrax Development

A fairly recent development in differential transmissions is called "quadrax." Here, four conductors are enclosed by a single shield. The conductors are diagonally paired to form two differential pairs with mutually perpendicular electric and magnetic fields, thus nearly eliminating all crosstalk. This has the advantage of size and cost reduction.

Quadrax is often used through longer line runs up to 30 m or more with equalization. However, conversion to separated twinax cables must occur at some point. Because a connector pair usually exists from the equipment panel to the internal circuitry, the conversion is best achieved within the connector receptacle. Direct wiring requires the conductors to cross over, causing an unwelcome and inconsistent impedance disturbance, even with short leads. This is acceptable for low data rates, but when the data rate equivalent frequency approaches microwave and the lead lengths become a significant portion of a wavelength, this method compromises system performance by producing reflections and crosstalk.

The Quadsplitter

A better solution to this problem is use of a built-in feature within the receptacle member of the connector pair. This feature effectively divides the quadrax inner conductors into two separate twinax paths without disturbing the impedance any more than a stripline surface-launch microwave coaxial connector. A "quadsplitter" accomplishes this goal by employing multilayer stripline circuit boards carrying short runs of paired strip conductors between ground planes. The attachment of the four contacts within the mating end of the connector is routed to the assigned circuit board while merely passing through the board assigned to the other pair. Figure 1 depicts a complete assembly using a MIL-C-38999 Series III size 11 receptacle with the rear cover removed. The twinax attachment is visible.

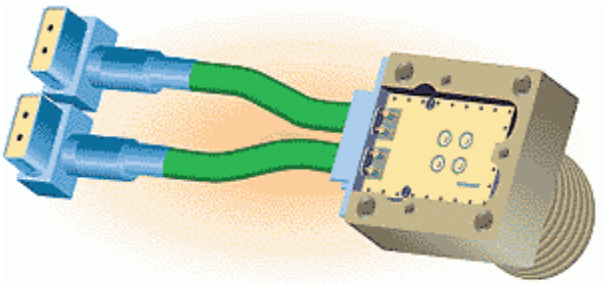


Figure 1. A fully compensated size 11 single quadrax assembly split into two twinax cables with rear cover removed.

Five layers are used to form the multilayer stripline circuit board (see Figure 2). By conductor coating one side of each board, three ground planes are established that provide two trace layers sandwiched between ground planes. Each trace accesses the surface region or board edge through conductor-coated holes. The region where the front contacts interface with the board surface requires considerable attention, as sudden changes in diameter produce fringing capacitance. In any case, compensating dimension adjustment is straightforward. This condition also exists at the board edge, which again can be compensated. The internal trace dimensions and ground plane separation is calculable from standard stripline equations or available finite element software.

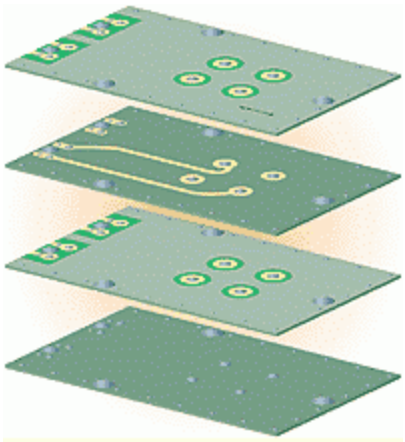


Figure 2. Five layers/four boards are used to form the multilayer stripline circuit board.

Sabritec has developed the “Quadsplitter” to meet the needs of current and future high-speed transmission systems. Sabritec has also developed in-house test capabilities to provide test data to our customers on the performance of our Fibre Channel connectors.

Below are detailed eye pattern and jitter test results for one “Quadsplitter” configuration tested at 1.0625 Gbps. Descriptions of the test equipment used and methods employed to test the “Quadsplitter” are also included. Test data to support higher data transmission rates can also be supplied upon request of the customer.

2 Time Domain Testing:

Eye Pattern, Jitter (UI p-p) and Jitter RMS Time Domain Reflectometry	ANSI Fibre Channel Physical Interface dpANS NCITS.xxx-200x XX-00-199x Physical Interface December 9, 2001 Defined per 100-DF-EL-S, Inter-Enclosure, Max.

3 Test Equipment and Facilities

3.1 Test Equipment

The following test equipment shall be used when testing is to be accomplished to the criteria of this specification. Equivalent items may be used if the effectiveness and accuracy of the tests are not adversely affected. Substitutes will be authorized by Sabritec Quality Assurance. Table #3 lists the equipment to be used during the performance of the testing required herein.

Table 1: Test Equipment

Manufacturer	Model and Description
Tektronix	CSA 8000, Communications Signal Analyzer
Tektronix	80E04, Electrical Sampling Module
Tektronix	AWG 610, Arbitrary Waveform Generator

3.2 Time Domain Testing

Eye Pattern Mask as follows: @ 1.0625 Gbps:

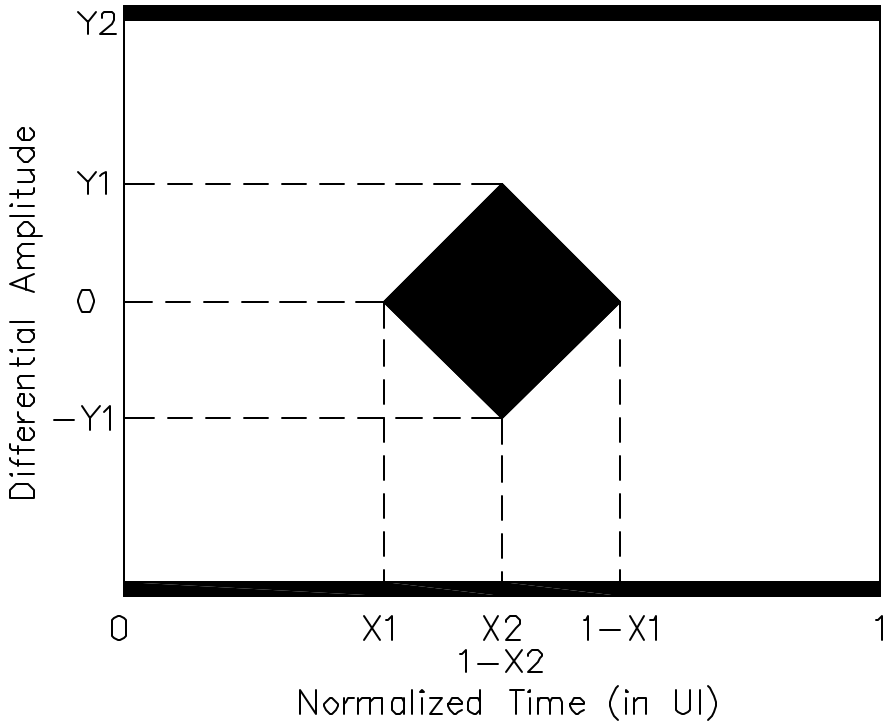


Figure 1 Eye Mask Data

Normalized Time Coordinates:

1 UI = (1/ 1.0625 Gbps)	= 941 pS
X1 = (1/2)(0.54)(941 pS)	= 254 pS
X2 = (1/2)(941 pS)	= 471 pS
1-X1 = (941 pS – 254 pS)	= 687 pS

4 Time Domain Reflectometry (TDR)

Time Domain Reflectometry is the analysis of a conductor (wire, cable, or fiber optic) by sending a pulsed signal into the conductor, and then examining the reflection of that pulse.

Sabritec uses the Tektronix Communications Signal analyzer CSA 8000 with the 80E04 Sampling Head.

The 80E04 is a dual-channel Time Domain Reflectometry (TDR) sampling module. This sampling module provides an acquisition rise time of 17.5 ps or less, with a typical 20 GHz equivalent bandwidth.

Each channel of the 80E04 is capable of generating a fast step for use in TDR mode and the acquisition portion of the sampling module monitors the incident step and any reflected energy. The reflected rise time of the TDR step is 35 ps or less and the polarity of each channel's step can be selected independently. This allows for differential or common-mode testing of two coupled lines, in addition to the independent testing of isolated lines.

Below is a plot of the impedance of the test fixture to show the open occurring at the end of the M38999 Connector:

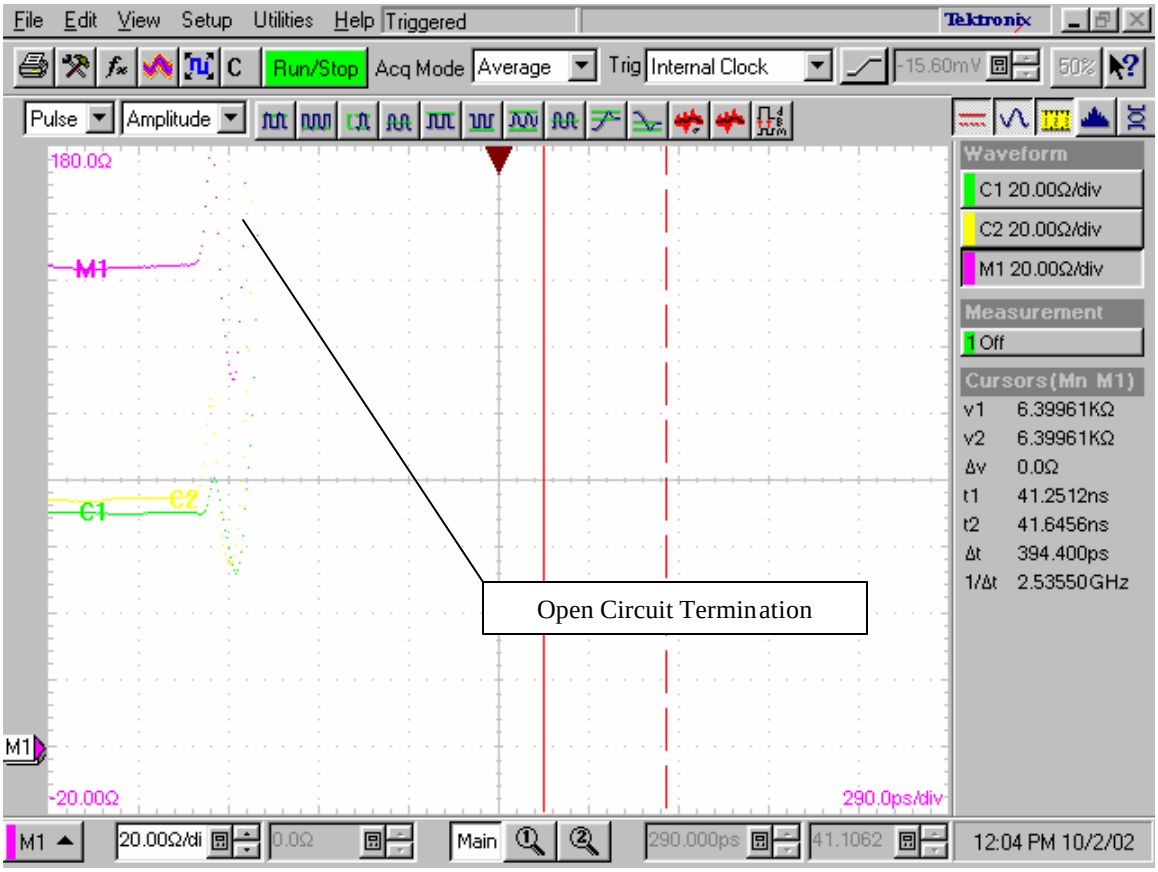


Figure 2 Open Circuit Termination Impedance

After connecting the mating Right Angle QuadSplitter Receptacle, the impedance can now be verified as shown below:

Each letter represents the approximate location of the trace as compared from graph to connector.

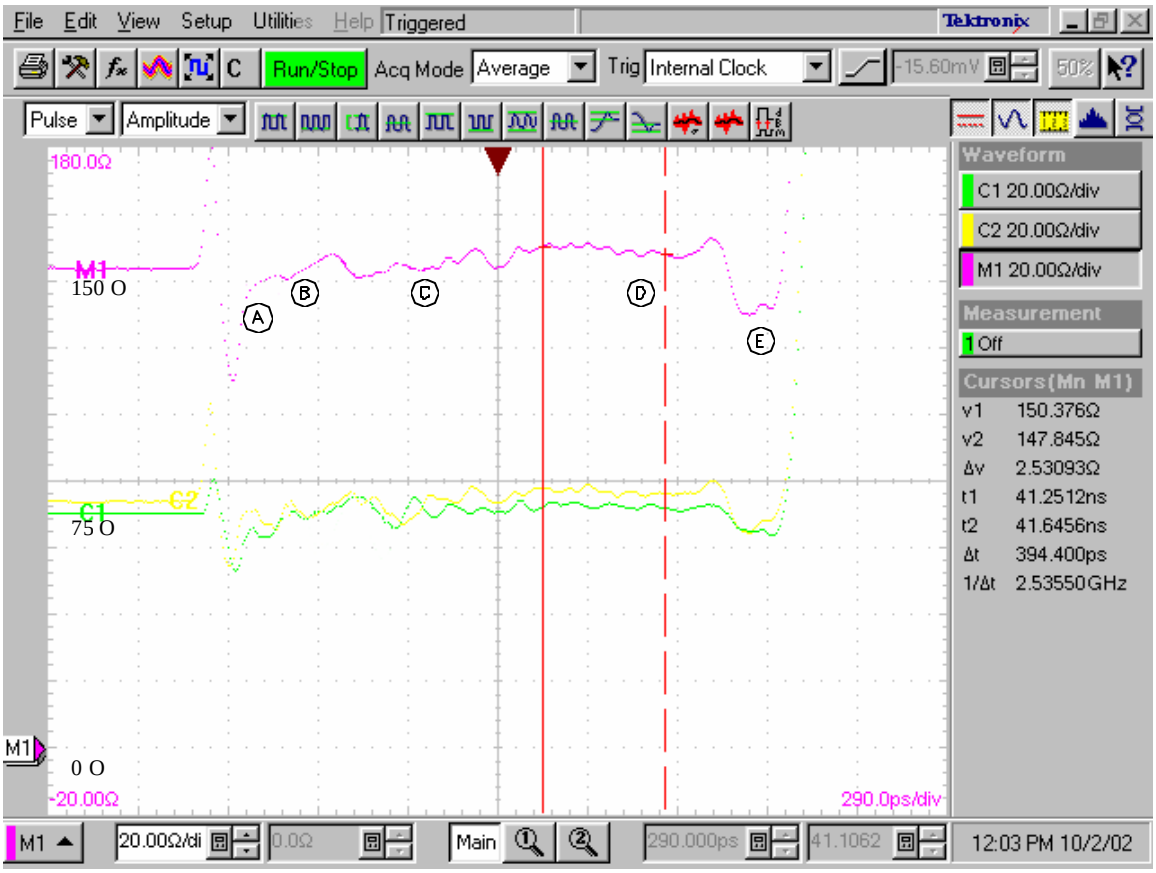
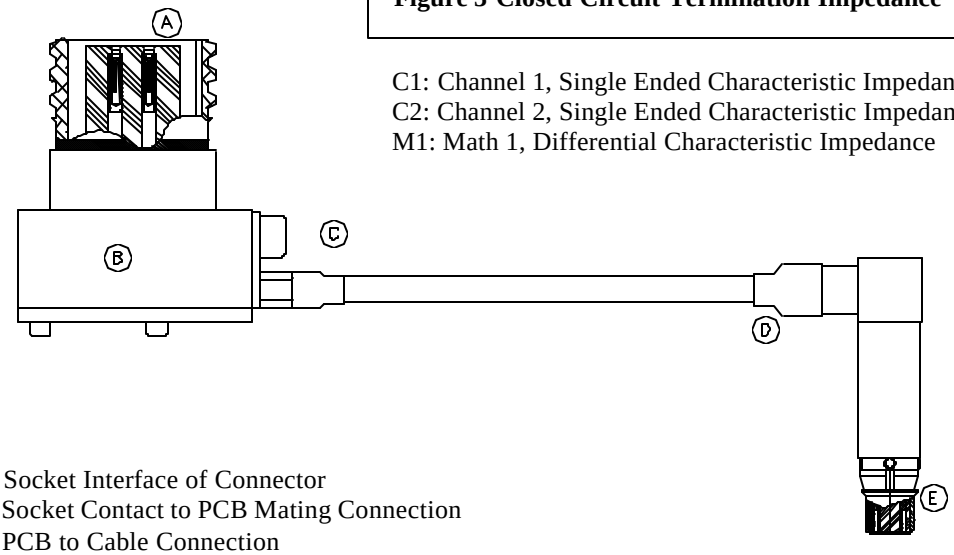


Figure 3 Closed Circuit Termination Impedance

C1: Channel 1, Single Ended Characteristic Impedance
C2: Channel 2, Single Ended Characteristic Impedance
M1: Math 1, Differential Characteristic Impedance



A: Socket Interface of Connector
B: Socket Contact to PCB Mating Connection
C: PCB to Cable Connection
D: Cable to Twinax Contact Connection
E: End of Twinax Contact, Open Circuit Termination

5 Eye Pattern and Jitter Testing @1.0625 Gbps

Eye pattern is defined as an oscilloscope display in which a pseudorandom digital data signal from a receiver is repetitively sampled and applied to the vertical input, while the data rate is used to trigger the horizontal sweep. Note: System performance information can be derived by analyzing the display. An open eye pattern corresponds to minimal signal distortion. Distortion of the signal waveform due to interference and noise appears as closure of the eye pattern.

Jitter is defined 52 as the deviation from the ideal timing of an event. The reference event is the differential zero crossing for electrical signals and the nominal receiver threshold power level for optical systems. Jitter is composed of both deterministic and Gaussian (random) content.

Sabritec uses the Tektronix Communications Signal analyzer CSA 8000 with the 80E04 Sampling Head to digitally store the pseudo random data. A Tektronix AWG 610 is used to drive the signal at 1.0625 Gpbs.

The AWG 610 generates predefined waveforms that simulate pseudo random bit streams (PRBS) for physical layer testing for the FC1063E standard.

A pseudorandom digital signal at 1.0625 Gbps was programmed into the AWG 610. Outputs on the front on the AWG 610 are differentially driven, with Channel 1 and Channel 1 Inverse. An impedance controlled stripline PCB is then used to connect the differential signal to the Twinax connector. A mating plug is then connected to the receptacle interface, which connects to the CSA8000. A picture of the test apparatus is shown below in Figure 4.

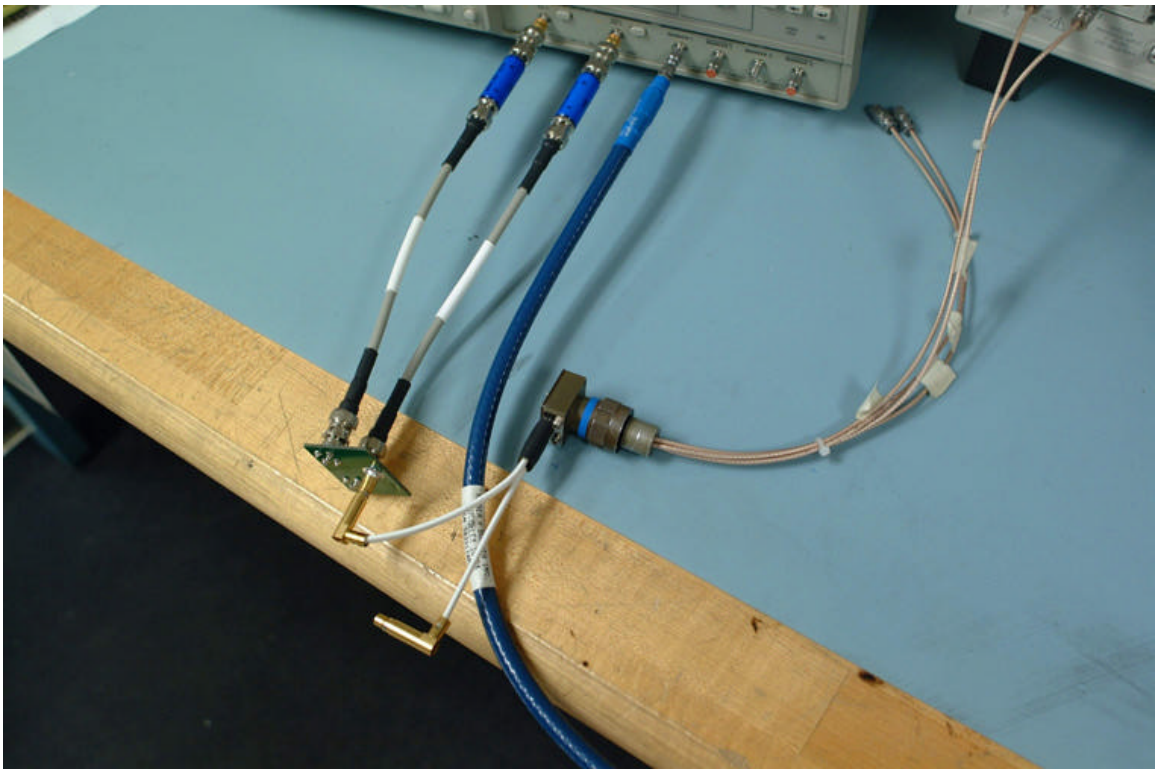


Figure 4 Test Connector and Related Wiring

Below, a 1.0625 Gbps NRZ signal is digitally stored with RMS Jitter, Peak to Peak Jitter, Eye Width, and Bite Rate.

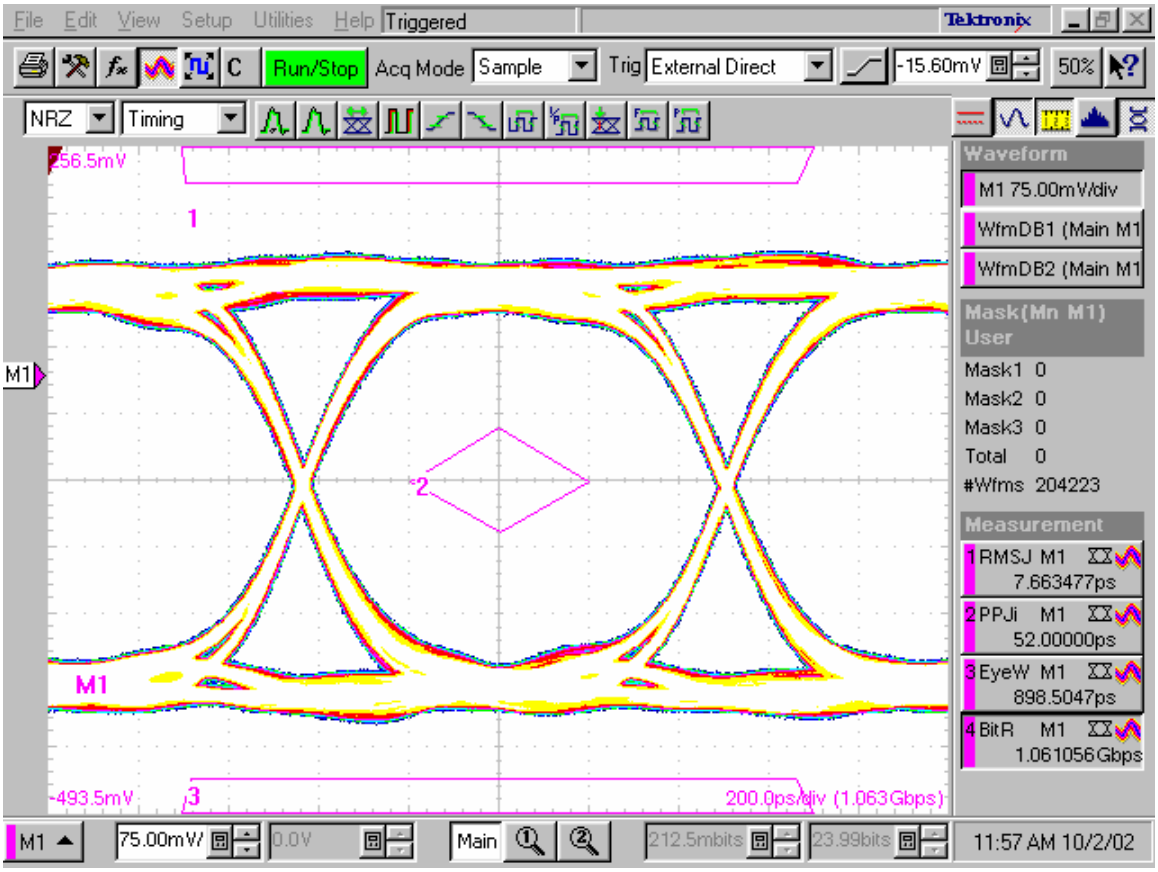


Figure 5 1.0625Gbps Eye Pattern Diagram

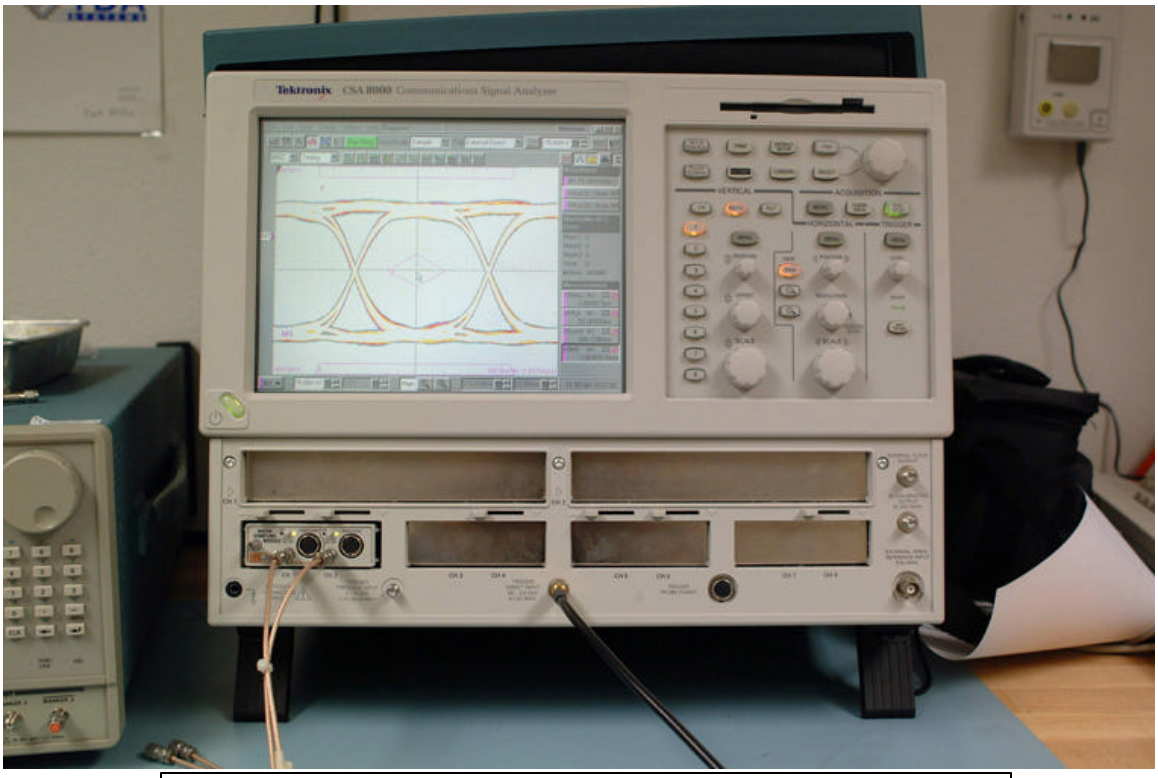


Figure 6 The Tekronix CSA 8000 with 80E04 Sampling Head

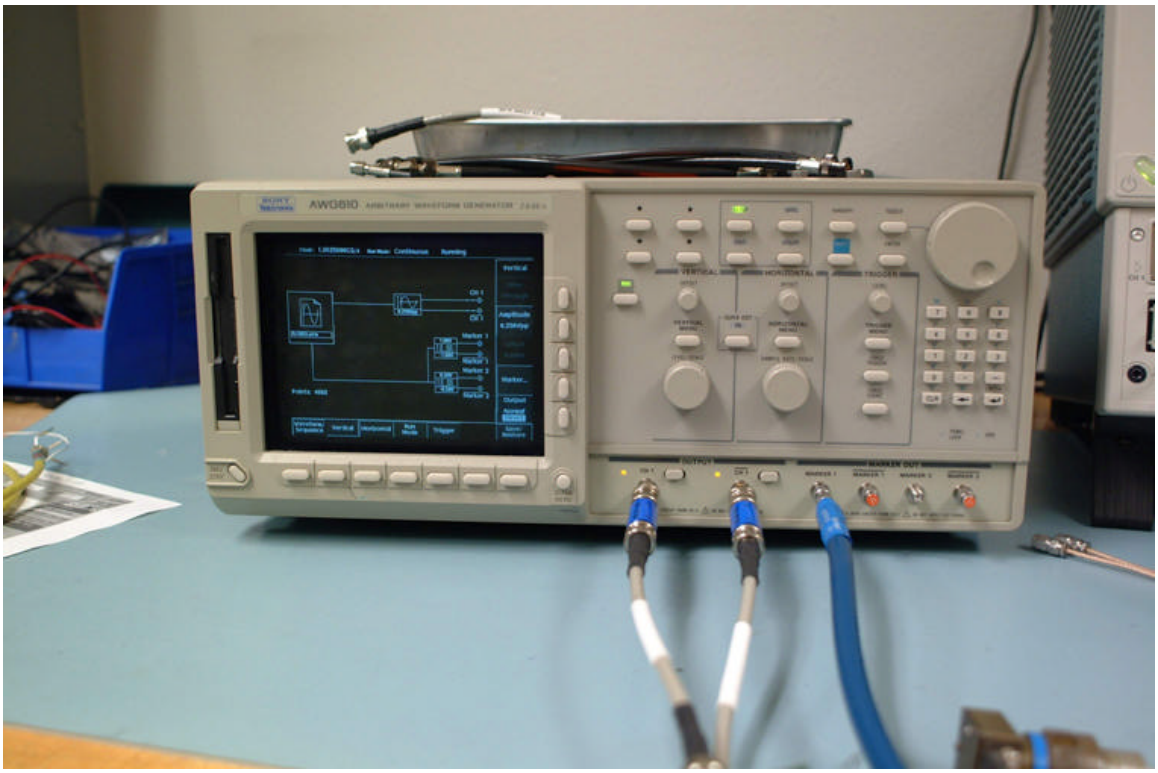
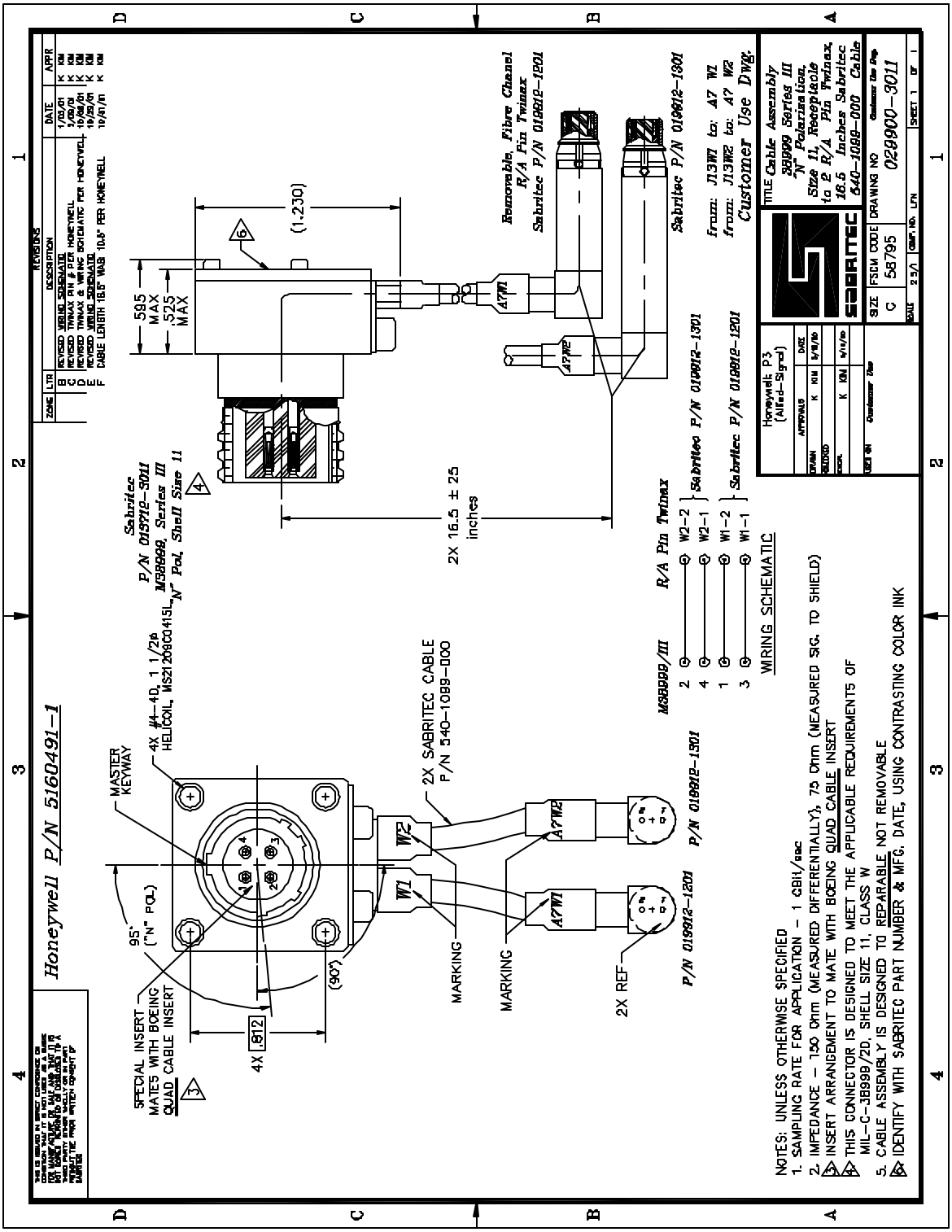


Figure 7 The AWG 610 Arbitrary Waveform Generator

6 Customer Drawing of Sabritec Part Number 029900-3011



7 Digital Domain Definitions:

α_T, α_R	Reference points used for establishing jitter budgets at the chip pins nearest the SERDES.
β_T, β_R	Reference points used for establishing jitter budget at the internal connector nearest the re-timing element.
δ_T, δ_R	Reference points used for establishing jitter budget at the internal user connector nearest the gamma point.
γ_T, γ_R	Reference points used for establishing jitter budgets at the external enclosure connector.
Baud	A unit of signaling speed, expressed as the maximum number of times per second the signal can change the state of the transmission line or other medium. (Units of Baud are sec^{-1}) Note: With the Fibre Channel transmission scheme, a signal event represents a single transmission bit. [(Adapted from IEEE Std 610.7-1995 [A16].12)].
Bit Error Rate (BER)	A parameter that reflects the quality of the serial transmission and detection scheme. The BER is calculated by counting the number of erroneous bits output by a receiver and dividing by the total number of transmitted bits over a specified transmission period. For example, a BER of 10^{-12} is one bit error received in 10^{12} bits transmitted. For a 1,0625 GBaud datastream, 10^{-12} bit error rate translates into an average of one bit error every 941 secs or one bit error every 16 minutes if the errors are occurring as isolated single events. For cases where the errors occur in bursts the temporal distribution must also be considered.
Bulkhead	The boundary between the shielded system enclosure (where EMC compliance is maintained) and the external interconnect attachment.
CDR	The function is provided by the SERDES circuitry responsible for producing a regular clock signal from the serial data and for aligning this clock to the serial data bits. The CDR uses the recovered clock to recover the data.
Compliance Points	Physical positions between transmit and receive integrated circuits where measurements are applied to determine if the properties satisfy the specification requirements. Interoperability between components attached at compliance points is expected if the specifications are met at the compliance points.
Component	Entities that make up the link. Examples are connectors, cable assemblies, transceivers, port bypass circuits and hubs.
Connectors	Electro-mechanical or opto-mechanical components consisting of a receptacle and a plug which provides a separable interface between two transmission media segments. Connectors may introduce physical disturbances to the transmission path due to impedance mismatch, crosstalk, etc. These disturbances can introduce jitter under certain conditions.
Coupler	A connector that mates two like media together.
Device	An entity that contains at least one Fibre Channel port. Examples are: host bus

	adapters, disk drives, and switches. Devices may have internal connectors or bulkhead connectors.
Duty Cycle Distortion (DCD)	Difference in the mean pulse width of a "1" pulse compared to the mean pulse width of a "0" pulse in a clock-like (repeating 0,1,0,1,...) bit sequence. DCD is part of the DJ distribution and is measured at the ideal receiver threshold point.
Enclosure	An outermost physical boundary surrounding one or more Fibre Channel ports that is intended to comply with EMI, safety, and other regulatory requirements.
Fibre Channel (FC)	A collection of physical technologies described in the referenced Fibre Channel standards documents.
Fill Word	An IDLE or ARB primitive signal. These words are transmitted between frames, primitive signals, and primitive sequences to keep a link active.
Gaussian	A statistical distribution (also termed "normal") characterized by populations that are not bounded in value and have well defined "tails". Analog amplifiers are the most important source of Gaussian noise in serial data transmissions. The term "random" in this document always refers to jitter that has a Gaussian distribution.
"Golden"	An adjective describing a component having exceptionally tight performance and calibration requirements.
Interconnect	The means for providing the path between the γ_T and γ_R compliance points. The interconnect may be as simple as a length of twinax or as complex as consisting of multiple components such as: connectors, active elements (e.g. PBC's and retimers), hubs, and board traces.
Intersymbol Interference (ISI)	Data dependent deterministic jitter caused by the time differences required for the signal to arrive at the receiver threshold when starting from different places in bit sequences (symbols). For example when using media that attenuates the peak amplitude of the bit sequence consisting of alternating 0,1,0,1... more than peak amplitude of the bit sequence consisting of 0,0,0,0,1,1,1,1... the time required to reach the receiver threshold with the 0,1,0,1... is less than required from the 0,0,0,0,1,1,1,1.... The run length of 4 produces a higher amplitude which takes more time to overcome when changing bit values and therefore produces a time difference compared to the run length of 1 bit sequence. When different run lengths are mixed in the same transmission the different bit sequences (symbols) therefore interfere with each other. ISI is expected whenever any bit sequence has frequency components that are propagated at different rates by the transmission media.
Jitter	The deviation from the ideal timing of an event. The reference event is the differential zero crossing for electrical signals and the nominal receiver threshold power level for optical systems. Jitter is composed of both deterministic and Gaussian (random) content.
Jitter, Data Dependent	The jitter which is added when the transmission pattern is changed from a clock like to a non-clock like pattern. Includes ISI.
Jitter, Deterministic	Jitter with non-Gaussian probability density function. Deterministic jitter is always bounded in amplitude and has specific causes. Four kinds of deterministic jitter are

	identified: duty cycle distortion, data dependent, sinusoidal, and uncorrelated (to the data) bounded. DJ is characterized by its bounded, peak-to-peak value.
Jitter Generation	The quantity of jitter added to an incoming signal by a component, device, system, or media. This term is not used in this document. See jitter output.
Jitter Output	The quantity of jitter at a specific physical position in the link.
Jitter, Peak-to-Peak	Peak For any type of jitter, the minimum, full range of the jitter values that excludes (includes all but) 10^{-12} of the total jitter population.
Jitter, Random	Random Jitter that is characterized by a Gaussian distribution. Random jitter is defined to be the peak-to-peak value which is given to be 14 times the standard deviation of the Gaussian distribution for a BER of 10^{-12}.
Jitter, RMS	The root mean square value or standard deviation of jitter. For a Gaussian distribution, the RMS value is 1/14 of the peak-to-peak value for BER 10^{-12}.
Jitter Tolerance for CDR	The ability of a CDR circuit to recover an incoming datastream correctly despite jitter. It is characterized by the amount of jitter required to produce a specified bit error rate. The reference point for jitter tolerance is the α_R point. The tolerance depends on the frequency content of the jitter. Since bit errors determine the tolerance, only devices capable of reporting bit errors may be used.
Jitter, Total	The sum of all random and deterministic jitter components.
Jitter Transfer	The ratio between the jitter output and jitter input for a component, device, or system often expressed in dB. A negative dB jitter transfer indicates the element removed jitter. A positive dB jitter transfer indicates the element added jitter. A zero dB jitter transfer indicates the element had no effect on jitter. The ratio should be applied separately to deterministic jitter components and Gaussian (random) jitter components. The concept of jitter transfer is not addressed in this document.
Jitter, Bounded and Uncorrelated	Deterministic jitter that is caused by other than the data on the signal under test.
Link	(1) A duplex serial data connection between two ports including the serializer, deserializer, PMD, connectors, and media. (as defined in FC-PH). (2) Two unidirectional fibres transmitting in opposite directions and their associated transmitters and receivers.
Media	(1) General term referring to all the elements comprising the interconnect. This includes fiber optic cables, optical converters, copper cables, pc boards, connectors, hubs, and port bypass circuits. (2) May be used in a narrow sense to refer to the material in cable assemblies that are not part of the connectors.
Physical Media Dependent	A transmit and receive network used to launch into a specific type of electrical or optical interconnect or to receive from a specific type of electrical or optical interconnect. The details of the network design depend on the type of interconnect.
Port (or FC Port)	A generic reference to a Fibre Channel Port. In this document, the components that together form or contain the following: the FC protocol function with elasticity buffers to re-time data to a local clock, the SERDES function, the

	transmit and receive network, and the ability to detect and report errors using the FC protocol.
Port Bypass Circuit	An active multiplexer which is used to bypass FC ports or other ports that are unused or nonfunctional. PBCs which do not re-time the signals to a local clock are considered part of the interconnect.
Random	Random in this document always refers to jitter that has a Gaussian distribution.
Receive Network	A receive network consists of all the elements between the connector inclusive of the connector and the deserializer or repeater chip input. This network may be as simple as a termination resistor and coupling capacitor or this network may be complex including components like photodiodes and transimpedence amplifiers.
Repeater	A circuit for receiving either one-way or two-way communication signals and delivering corresponding signals which are either amplified, reshaped, or both. Repeaters are characterized by their jitter transfer. In the context of fibre channel jitter methodology, the repeater could be a simple amplifier or a serial-data-in and serial-data-out component that modifies jitter by re-generating the serial data edges to a defined timing relation with a recovered bit clock.
Retimer	A circuit that retransmits buffered FC data and whose transmit clock is derived from a timing reference other than the received data. A retimer shall be capable of inserting and removing fill words. In the context of fibre channel jitter methodology, a retimer resets the accumulation of jitter in a link so that the output of a retimer has the jitter budget of αT.
SERDES	SERializer and DESerializer function. An example of Fibre Channel deployment is based on a SERDES function with I/O functional and timing definitions as specified in the "10-Bit Interface Specification." The CDR function is included in the deserializer.
Transmit Network	A transmit network consists of all the elements between a serializer or repeater output and the connector inclusive of the connector. This network may be as simple as a pulldown resistor and ac capacitor or this network may include laser drivers and lasers.
Unit Interval	One nominal bit period for a given signaling speed. It is equivalent to the shortest nominal time between signal transitions. UI is the reciprocal of Baud (Units of UI are seconds)
Wander	Long term deviation of the data rate frequency of a digital signal. Wander typically refers to frequency deviation occurring at rates of less than 10 Hz.